light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

gate control lines connected to gate electrode groups in which horizontal lines belonging to each coset of modulo N within successive pixel rows are connected commonly, N being a predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, being combined with each other so as to reduce the number of the connection terminals to less than N.

Please replace claim 3 with the following:

3. (TWICE AMENDED) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes being provided in a predetermined number N of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N, N being a predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number corresponding to the periodic unit about connections to said connection terminals within said successive pixel rows, some of the gate electrode groups being commonly connected so that the connection terminals are less in number than N.

Please replace claim 4 with the following:

4. (TWICE AMENDED) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates;

and a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes making up N of gate electrode groups in which the lines belonging to each coset of modulo N within successive pixel rows are connected to common lead lines, N being a predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, the gate electrode groups having common connections to reduce the number of the connection terminals to less than N,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

Please replace claim 5 with the following:

5. (TWICE AMENDED) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

gate control lines connected to gate electrode groups in which the horizontal lines belonging to each coset of modulo N within successive pixel rows are connected commonly, N being a predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, being combined with each other so as to reduce the number of the connection terminals to less than N,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

Please replace claim 6 with the following:

6. (TWICE AMENDED) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes being provided in a predetermined number N of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N, N being a predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number corresponding to the periodic unit about connections to said connection terminals within successive pixel rows, some of the gate electrode groups being commonly connected so that the connection terminals are less in number than N,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

Please cancel claim 10 without prejudice to, or disclaimer of, the subject matter recited therein.

Please add the following new claim:

--11. (NEW) A solid-state imaging device comprising:

a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, and a plurality of R gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

wherein the R gate electrodes are divided into S gate groups, each gate group having R/S gate electrodes,

wherein the R gate electrodes are divided into R/S pixel groups, each having R/(R/S) consecutive, adjacent, gate electrodes,

wherein the i^{th} gate electrode of each pixel group, where i = 1 to R/(R/S), share a common connection terminal, and

wherein at least two gate electrodes within a given pixel group share a common connection terminal.--

In accordance with 37 C.F.R. § 1.121(c)(1)(ii), separate sheets with the rewritten claims marked-up to show